REMARKS / ARGUMENTS

The present application includes pending claims 1-15, all of which have been rejected. The Applicant respectfully submits that the claims define patentable subject matter.

Initially, the Applicant notes that a goal of patent examination is to provide a prompt and complete examination of a patent application.

> It is essential that patent applicants obtain a prompt yet complete examination of their applications. Under the principles of compact prosecution, each claim should be reviewed for compliance with every statutory requirement for patentability in the *initial review* of the application, even if one or more claims are found to be deficient with respect to some statutory requirement. Thus, Office personnel *should* state *all* reasons and bases for rejecting claims in the *first* Office action. Deficiencies should be explained clearly, particularly when they serve as a basis for a rejection. Whenever practicable, Office personnel should indicate how rejections may be overcome and how problems may be resolved. A failure to follow this approach can lead to unnecessary delays in the prosecution of the application.

See Manual of Patent Examining Procedure (MPEP) § 2106(II). As such, the Applicant assumes, based on the goals of patent examination noted above, that the present Office Action has set forth "all reasons and bases" for rejecting the claims.

Claims 1, 8-9, 12 and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,356,497, issued to Puar et al.

(hereinafter, Puar), in view of U.S. Patent No. 6,395,591, issued to McCormack et al. (hereinafter, McCormack). Claims 1-10, 12 and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack in view of Puar. Claims 11 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack and Puar as applied to claim 1, and further in view of U.S. Patent No. 6,403,992, issued to Wei (hereinafter, Wei). Claims 1-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wei in view of Puar. The Applicant respectfully traverses these rejections at least for the reasons previously set forth during prosecution and at least based on the following remarks.

REJECTION UNDER 35 U.S.C. § 103

In order for a *prima facie* case of obviousness to be established, the Manual of Patent Examining Procedure ("MPEP") states the following:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the teaching. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (emphasis added)

See MPEP at § 2142, citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added). Further, MPEP § 2143.01 states that "the mere fact that

references can be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination," and that "although a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be *a suggestion or motivation in the reference* to do so'" (citing In re Mills, 916 F.2d 680, 16 USPQ 2d 1430 (Fed. Cir. 1990)). Moreover, MPEP § 2143.01 also states that the level of ordinary skill in the art cannot be relied upon to provide the suggestion...," citing Al-Site Corp. v. VSI Int'l Inc., 174 F.3d 1308, 50 USPQ 2d 1161 (Fed. Cir. 1999). Additionally, if a *prima facie* case of obviousness is not established, the Applicant is under no obligation to submit evidence of nonobviousness.

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

I. The Proposed Combination of Puar and McCormack Does Not Render Claims 1-10, 12 and 14-15 Unpatentable (Pages 2-4 of the Final Office Action)

The Applicant first turns to the rejection of claims 1-10, 12 and 14-15 as being unpatentable over Puar in view of McCormack.

A. Rejection of Claim 1

With regard to the rejection of independent claim 1 under 103(a), the Applicant submits that the combination of Puar and McCormack does not disclose or suggest at least the limitation of "a shielding layer, wherein said shielding layer reduces transfer of noise in the chip," as recited by the Applicant in independent claim 1. The Final Office Action states:

> Puar (Fig. 5) discloses a system for reducing noise in a chip, the system comprising: a substrate layer (P substrate) integrated within the chip; a transistor well layer (N-Well) integrated within the chip; at least one transistor of a first transistor type (P-type) formed within the well layer; and a positive potential of a quiet voltage source Vdd (column 4, lines 59-63) that is coupled to the at least one transistor of the first transistor type.
>
> **Puar does not disclose that the transistor well layer (N-Well) is shielded by a shielding layer.**
>
> However, McCormack (Fig. 2) teaches the forming of a transistor within a transistor well layer and on a lightly doped (p-) substrate layer 50. The transistor well layer is isolated or shielded from the substrate 50 by a p type epitaxy layer 12 disposed therebetween. **The layer 12 functions as a shielding layer for reducing the noise in the chip because it isolates the substrate 10 from the transistor layer and has a higher doping than the underlying substrate 10 for providing immunity against parasitic substrate effects or latchup effects (column 1, lines 19-24 and column 4, lines 9-13).** Accordingly , it would have been obvious to modify the device of Puar by forming the shielding layer between the substrate layer and the transistor well layer because such forming of the low resistivity shielding layer would isolate the noise transfer to the transistor layer by reducing parasitic substrate effects or latchup effects. (emphasis added)

See the Final Office Action at pages 2-3. The Applicant submits that the above bolded statement by the Examiner, namely that "**layer 12 ... has a higher**

doping than the underlying substrate 10 for providing immunity against parasitic substrate effects or latchup effects" is completely erroneous and is not supported by McCormack. The Examiner seeks support in column 1, lines 19-24 and column 4, lines 9-13 of McCormack.

> McCormack states the following at col. 1, lines 19-24:
>
> While a lightly doped p-type substrate having a resistivity of 5 or 20 ohm-cm has been used in early fabrication processes, this was found to be problematic for CMOS integrated circuits because the high substrate resistance renders the integrated circuit more susceptible to latchup.

First of all, *this citation of McCormack is taken from the BACKGROUND section of McCormack* and it clearly does not relate to any elements disclosed by McCormack. The Applicant is confused as to why the Examiner is citing from the BACKGROUND section without any support whatsoever that any of the cited material relates to layer 10, layer 12 or, for that matter, to any other element of the invention of McCormack.

> McCormack states the following at col. 4, lines 9-13:
>
> A conventional way to reduce latchup susceptibility is to lower the resistance of the P-wells. A low P-well resistance has the effect of decoupling the parasitic bipolar transistors formed by the source/drain regions and the n and p tubs in a CMOS process.

The Applicant is, again, confused as to why the Examiner is citing col. 4, lines 9-13 as this citation of McCormack relates to the resistance of the p-wells and it does not relate in any way to the doping of layers 10 or 12.

Therefore, **the McCormack reference does not disclose or suggest that the p type layer 12 has higher doping than the lightly doped (p-) substrate 10. In fact, McCormack teaches away from the notion that layer 12 has higher doping than layer 10 as McCormick discloses that the resistance for both the p-type substrate 10 and the p-type epi-layer 12 are in the same 14-28 ohm-cm range.** *See* McCormack, col. 5, lines 45-47 and col. 6, lines 1-3.

Furthermore, nowhere in the McCormack reference is there any claim or inference that the p-type epitaxy layer 12 functions as a "shielding layer." McCormack **credits the enhanced circuit performance while offering protections against parasitic effects to the heavily doped p++ region 14, not to the p type epitaxial layer 12.** McCormack discloses a selective substrate implant process that "is capable of enhancing the circuit performance while offering protections against parasitic effects" (Column 2, Lines 57-59) by forming "a heavily doped p++ region 14," (Column 2, Lines 65-66) that is "formed only in areas where P-wells are to be built." (Column 6, Lines 43-44). **Even if the heavily doped p++ region 14 in McCormack functions as a "shielding" region, the heavily doped p++ region 14 in McCormack can not function as a shielding layer since it only covers a portion of the substrate layer.** In fact,

not only does McCormack fail to disclose a "shielding layer," **McCormack actually teaches away from a "shielding layer."** In Column 6, Lines 40-44, McCormack states that "one having ordinary skilled in the art would understand that the heavily doped regions are formed only in areas where P-wells are to be built." (Emphasis added).

As shown above, neither Puar nor McCormack teach or suggest the limitation of "a shielding layer, wherein said shielding layer reduces transfer of noise in the chip," as recited by the Applicant in independent claim 1. For at least the reasons set forth above, the Applicant respectfully asserts that claim 1 is allowable over McCormack and Puar. The Applicant requests that the rejection of claim 1 be withdrawn.

B. Rejection of Dependent Claims 2-10, 12 and 14-15

Based on at least the foregoing, the Applicant believes the rejection of independent claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Puar in view of McCormack has been overcome and requests that the rejection be withdrawn. Additionally, since the additional cited references do not overcome the deficiencies of McCormack, claims 2-10, 12 and 14-15 depend from independent claim 1, respectively, and are, consequently, also respectfully submitted to be allowable.

The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 1-10, 12 and 14-15.

II. The Proposed Combination of McCormack, Puar and Wei Does Not Render Claims 11 and 13 Unpatentable

Claims 11 and 13 depend from independent claim 1. Since Puar and Wei do not cure the deficiencies of McCormack, the Applicant submits that claims 11 and 13 are allowable at least for the reasons stated above with regard to allowability of claim 1. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 11 and 13.

III. The Proposed Combination of Wei and Puar Does Not Render Claims 1-13 Unpatentable

The Applicant now turns to the rejection of claims 1-13 as being unpatentable over Wei in view of Puar.

A. Rejection of Claim 1

With regard to the rejection of independent claim 1 under 103(a), the Applicant submits that the combination of Wei and Puar does not disclose or suggest at least the limitation of "at least one transistor of a first transistor type that

couples said transistor layer to said shielding layer," as recited by the Applicant in independent claim 1. The Final Office Action states:

> Wei (Fig . 4) discloses a system for reducing noise in a chip, the system comprising: a substrate layer integrated within the chip; a transistor layer 46 integrated within the chip, which is shielded from the substrate layer by a shielding layer N-well 484, wherein the shielding layer N-well 484 reduces the transfer of noise or body effect in the chip (column 1, lines 55-60); **a transistor G4 of a first transistor type (p type) that couples the transistor layer 46 to the shielding layer 484**; and a positive potential Vcc (+5V) of a voltage source coupled to the transistor G4. (emphasis added)

See the Final Office Action at page 5. With regard to the above bolded portion of the Examiner's argument, the Applicant points out that item G4 designates a ground terminal for the PMOS transistor that is next to the NMOS transistor 46 (note that the PMOS transistor of Wei is not numbered in Figure 4, but it is numbered 52 in Figure 5). In this regard, G4 of Wei does not designate a "transistor". Furthermore, as illustrated in Figure 4 of Wei, Wei does not disclose or suggest any transistor that couples a transistor layer of any of the PMOS or NMOS 46 with the alleged shielding layer 484. Therefore, the Applicant submits that the combination of Wei and Puar does not disclose or suggest at least the limitation of "at least one transistor of a first transistor type that couples said transistor layer to said shielding layer," as recited by the Applicant in independent claim 1. Accordingly, the proposed combination of Wei and Puar does not render independent claim 1 unpatentable, and a *prima facie* case of obviousness has not

been established. The Applicant submits that claim 1 is allowable at least for the above reasons.

B. Rejection of Dependent Claims 2-13

Based on at least the foregoing, the Applicant believes the rejection of independent claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Wei in view of Puar has been overcome and requests that the rejection be withdrawn. Additionally, claims 2-13 depend from independent claim 1, respectively, and are, consequently, also respectfully submitted to be allowable at least for the above reasons.

The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 1-13.

IV. Reply to Office Action's Response To Arguments

The Final Office Action states the following:

> Regarding the rejections on claims 1-10, 12 and 14-15, Applicant asserts that "since epitaxial substrates have a low bulk resistivity material underneath the epitaxial layer, the epitaxial layers will couple noise more efficiently to nearby circuits or layers". Applicant then concludes that the epitaxial layer 12 of McCormack does not function as a shielding layer.
>
> This argument is not persuasive because of the following reasons:
>
> **First**, it is noted that the statement asserted by Applicant above is clearly applied when the substrate underneath the epitaxial layer

> has a resistivity lower than the resistivity of the epitaxial layer. However, it is not applied to the substrate and the epitaxial layer of McCormack because the substrate 10 does not have a resistivity lower than the resistivity of the epitaxial layer 12, but rather, the substrate 10 has a resistivity higher than the resistivity of the epitaxial layer 12 because the substrate 10 (P-) has lower doping than the epitaxial layer 12 (P);
>
> **Second**, McCormack states that "the high substrate resistance renders the integrated circuit more susceptible to latchup" (column 1, lines 22-24), and further states that "A conventional way to reduce latchup susceptibility is to lower the resistance of the P-wells" (column 4, lines 8-10). Accordingly, the forming of the layer 12 between the well layers and the substrate 10 would reduce the parasitic resistance effects and the parasitic capacitance effects formed between the well layers and the substrate 10 because the layer 12 (P-doping) shields the well layers from the substrate 10 and has a, resistivity lower than the resistivity of the substrate 10 (P doping). Therefore, the layer 12 is a shielding layer for reducing the noise in the chip because it has properties of enhancing latchup suppression formed between the well layers and the high resistivity substrate 10.

See the Final Office Action at pages 6-7 (emphasis added). Apparently, the entire reasoning in the Examiner's argument above is based on the assertion that somehow the substrate 10 has lower doping than the epitaxial layer 12, which results in higher resistivity of layer 12. As already explained above with regard to Section I-A of this response, as well as in previous Office Action responses, this assertion by the Examiner is false. **To reiterate, the Applicant points out that there is simply no support in McCormack that layer 10 has lower doping than layer 12. There is also no support in McCormack that layer 12 has lower resistivity than layer 10. On the contrary, McCormack explicitly**

discloses that layers 10 and 12 each have the same resistivity, namely 14-28 ohm-cm. Therefore, the Applicant maintains that claims 1-15 are allowable over the references cited in the Final Office Action.

CONCLUSION

Based on at least the foregoing, the Applicant believes that all claims 1-15 are in condition for allowance. If the Examiner disagrees, the Applicant respectfully requests a telephone interview, and requests that the Examiner telephone the undersigned Attorney at (312) 775-8176.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

A Notice of Allowability is courteously solicited.

Respectfully submitted,

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